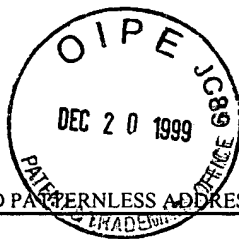


AMENDMENT AND RESPONSE

Serial Number: 08/984,560

Filing Date: December 3, 1997

Title: MEMORY DEVICE WITH PATTERNED AND PATTERNLESS ADDRESSING (as amended)



Page 2  
Dkt: 303.623US2

**IN THE ABSTRACT**

In the abstract, line 16, after the period, add the following sentence:

Additionally, a memory device switchable between a patterned and a patternless addressing scheme is provided.

**IN THE CLAIMS**

Please add claims 59-61 as follows:

59. (New) A memory device, comprising:  
a memory array;  
control logic operatively connected to the memory array, the control logic for selecting between a unpatterned pipeline and a patterned burst data pattern for accessing the memory array; and  
switching circuitry for switching between a first pathway and a second pathway depending on which of said pipeline scheme and said burst scheme is selected.

60. (New) A memory device, comprising:  
a memory array operable in a burst or a pipeline mode of operation;  
control logic for selecting between the burst or the pipeline mode of operation; and  
switching circuitry for switching between a first, burst data pathway and a second, pipeline data pathway depending on which of the burst or pipeline modes of operation is selected.

61. (New) A dynamic random access memory, comprising:  
a plurality of addressable memory arrays;  
a column address decoder for receiving an external column address;  
control logic for selecting between a burst or a pipeline mode of operation based;  
switching circuitry for switching between a burst pathway and a pipeline pathway depending on which of the burst or pipeline modes of operation is selected.

RECEIVED  
DEC 22 1999  
TECH CENTER 2700